REMARKS

Applicant thanks the Examiner for the careful review of this application. The specification was amended to correct a priority claim. An annotated sheet showing drawing changes as well as a replacement page is located at Appendix A of this paper. Claim 28 was canceled without prejudice and claims 7, 27 and 32 were amended to clarify aspects of the present invention. Additionally, claim 24 was amended to correct a clerical error. No new matter was added. Therefore, claims 1-27 and 29-34 are currently pending in this application.

DRAWING OBJECTIONS

The drawings were objected to because the schematic shown in figure 5 does not appear to correspond to the block diagram of figure 4. Specifically, the output sink network 302, as shown in figure 4, is coupled to V_{IN} while the output sink network 302 as shown in figure 5 is not directly coupled to V_{IN}. Applicant respectfully traverses.

As stated on page 8, line 17 of the specification, "figure 5 is a schematic of an output stage 500, *in accordance with one aspect of the present invention*," (emphasis added). Conversely, figure 4 depicts an output stage 400. In other words, figure 5 is not an expanded schematic of the block diagram of figure 4, as figure 4 depicts an output stage 400 and figure 5 depicts an output stage 500. Therefore, the output sink network 302, as shown in figure 5, is not meant to be coupled to V_{IN} as it is shown in a different embodiment than the one shown in figure 4.

However, a review of figure 5 revealed that the gates of transistors 502 and 402 need to be coupled to V_{IN} in order for the output stage 500 to function properly. Otherwise, the gates of transistors 402 and 502 are floating. As such, an annotated sheet showing changes as well as a replacement page of figure 5 can be found at Appendix A of this paper.

Withdrawal of the drawing objections and entry of the replacement figure 5 are respectfully requested.

CLAIM OBJECTIONS

Claims 24 and 25 were objected to under 37 C.F.R. § 1.75(c) as being in improper form "because a multiple dependent claims 23,13." Applicant assumes that the Examiner is objecting to claims 24 and 25 as being dependent from a multiple dependent claim, specifically claims 13 and 23. Applicant respectfully traverses for the following reasons.

A clerical error was removed from claim 24 by way of the preceding amendment. The amendment of claim 24 was not executed for the purposes of patentability, but rather to place it in better form for examination.

Withdrawal of the objections of claims 24 and 25 is respectfully requested.

REJECTIONS UNDER 35 U.S.C. § 112, SECOND PARAGRAPH

Claim 7 was rejected under 35 U.S.C. § 112, second paragraph for not particularly pointing out and distinctly claiming the subject matter which the Applicant regards as his invention. Specifically, the limitation "in the first field" lacks antecedent basis. The limitation "in the last field" has been amended to --in the first field effect device--.

Withdrawal of the rejection of claim 7 is respectfully requested.

REJECTIONS UNDER 35 U.S.C. § 102(b)

Claims 1, 3-11, 13-23 and 26-34 were under 35 U.S.C. § 102(b) as being anticipated by Dasgupta (U.S. Patent No. 5,900,783). Applicant respectfully traverses for the following reasons.

Dasgupta apparently discloses a circuit for a complimentary metal oxide semiconductor (CMOS) operational amplifier output stage which can possibly be connected easily to almost any input stage design and which can perhaps be coupled directly to that input stage. The circuit uses nine relatively small transistors and two output transistors. The output transistors are connected in series between the power supply rails and the size of the two output transistors determines the

current available to the load. The circuit of the invention can perhaps provide rail-to-rail output voltage swings and can perhaps drive a low ohm resistive load.

The invention as defined in independent claims 1, 11, 19, 27 and 32 is directed to an output stage, a method for providing an output signal, an ASIC and an amplifier output stage wherein the output stage that has an output sink network which drives the second field effect device such that a product of a first current in the first field effect device and a second current in the second field effect device is substantially equal to a predetermined constant. Applicant respectfully submits that Dasgupta does not disclose or reasonably suggest this limitation. In addition, this claim element was not addressed by the Examiner.

Furthermore, one skilled in the art would be dissuaded from using Dasgupta as a reference to achieve the present invention. Dasgupta's circuitry requires a bias network 26 of two stacked NMOS devices (205 and 206) to control the quiescent current of the output stage. This limits its lowest supply voltage to 1.8V or above. Advantageously, the present invention operates down to 0.9V. Additionally, the present invention also maintains a linear relationship between currents in NMOS transistor 404 and PMOS transistor 402 - this allows from improved linearity from the output stage and no crossover distortion, a feature not found in Dasgupta.

Claims 3-10, 13-18, 22-23, 26, 28-31 and 33-34 depend directly or indirectly from independent claims 1, 11, 19, 27 and 34 respectively and are therefore allowable for at least the same reasons as set forth for independent claims 1, 11, 19, 27 and 34. Withdrawal of the rejections of claims 1, 3-11, 13-23 and 26-34 is respectfully requested.

REJECTIONS UNDER 35 U.S.C. § 103(a)

Claims 2 and 12 were rejected as being unpatentable under 35 U.S.C. § 103(a) over Dasgupta (U.S. Patent No. 5,900,783). Applicant respectfully traverses for the following reasons.

Dasgupta was previously summarized. For reasons similar to those presented for independent claims 1 and 11, Applicant respectfully submits that claims 2 and 12 are also allowable as claims 2 and 12 depend from claims 1 and 11.

Withdrawal of the rejections of claims 2 and 12 are respectfully requested.

REJECTIONS UNDER 35 U.S.C. § 102(e)

Claims 1-34 were rejected under 35 U.S.C. § 102(e) as being anticipated by Stockstad (U.S. Patent No. 6,353,363). Applicant respectfully traverses for the following reasons.

Via the preceding amendment of the specification, the claim of priority to U.S. Patent No. 6,353,363 was corrected. Since the inventor (Troy Stockstad) of the present invention is the same as U.S. Patent No. 6,353,363 , Applicant respectfully submits that the '363 patent does not constitute prior art in relation to the present application. A terminal disclaimer is included with this paper in the event one is required to overcome any future, possible double patenting rejection.

Withdrawal of the rejections of claims 1-34 is respectfully requested.

The amendment was made to expedite the prosecution of this application. Applicant respectfully traverses the rejections of the originally submitted and previously amended claims and reserves the right to re-introduce them and claims of an equivalent scope in a continuation application. If the undersigned agent has overlooked a relevant teaching in any of the references, the Examiner is requested to point out specifically where such teaching may be found.

CONCLUSION

Applicant believes that all pending claims are allowable and a Notice of Allowance is respectfully requested.

If the Examiner believes that a conference would be of value in expediting the prosecution of this application, he is cordially invited to telephone the undersigned counsel at the number set out below.

Respectfully submitted,

PERKINS COIE LLP

Jonathan P. Kudla

Jonathan P. Kudla
Reg. No. 47,724

Customer No. 22918
Perkins Coie LLP
P.O. Box 2168
Menlo Park, CA 94026
Telephone: (650) 838-4300

APPENDIX A - DRAWINGS

Attorney Docket No. 54118-8004.US02

Annotated Sheet Showing Changes
10/006,924

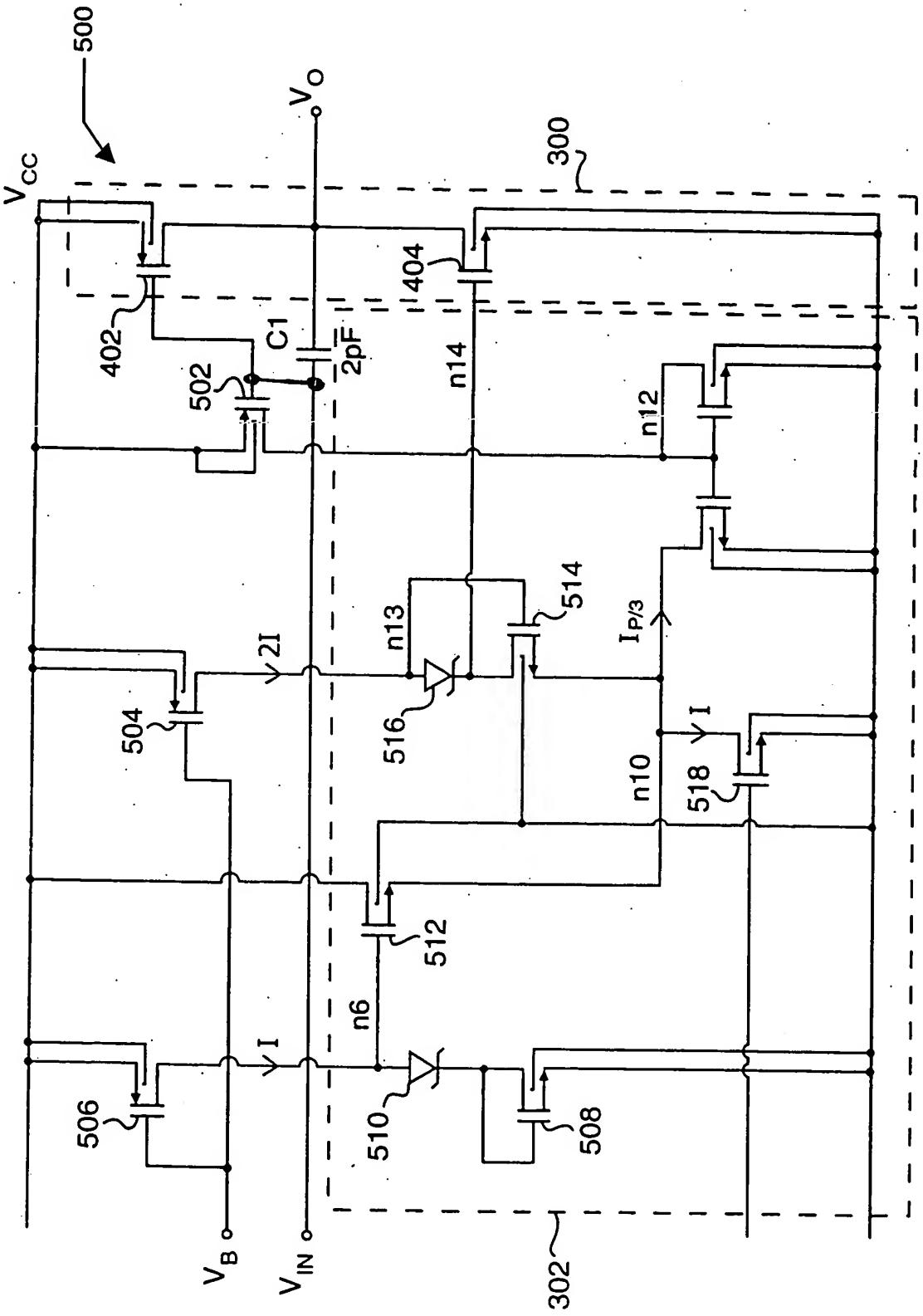

Fig. 5